REMARKS/ARGUMENTS

Status of Application

Claims 1-42 are pending in the present application. Claims 1-21, 23-25, 27-30, 32-34, 36-38 and 41 are rejected under 35 U.S.C. 102 (b). Claims 22, 26, 31, 35, 39 and 42 are rejected under 35 U.S.C. § 103. Claims 4, 29-32 and 37-40 are cancelled, rendering rejection to these claims moot.

Rejection under 35 USC § 102(b)

Claims 1-21, 23-25, 27-30, 32-34, 36-38 and 41 are rejected under 35 U.S.C. 102(b) as being anticipated by Bai, US 6,204,103. Applicants respectfully disagree.

All independent claims (1, 10, 16, 41 and 42) recite either method, IC or a gate electrode in which the gate electrode has a work function close to about a mid-gap of the silicon band. Claims 10 and 42 recite a gate electrode having a first material and metal wherein all of the first material and substantially all of the metal have been consumed during a reaction. Claims 1, 16 and 42 recites a gate layer having a first thickness t_p and a metal layer thereover having a thickness t_m, wherein the layers have a predetermined thickness ratio of t_m/t_p to result in all of the material of the gate layer and substantially all of the metal of the metal layer being consumed during reaction with one another. Claims 16 and 41 further require that problems associated with inversion and agglomeration from the formation of the transistor are reduced.

Bai, describes a method of forming a pair of NMOS and PMOS transistors. In particular, the NMOS and PMOS transistors have different work functions to optimize performance of the transistors. *See* Bai, col. 2 at lines 16-22. The NMOS transistor operates at a Fermi level near the conduction band (i.e., 4.1 eV) while PMOS transistor operates at a Fermi level near the valence band (i.e., 5.1 eV). *See* Bai, col. 5 at lines 37-51. Applicants submit that Bai nowhere

teaches forming a transistor having a mid-gap of the silicon band. In fact a mid-gap would be somewhere between 4.1 eV and 5.1 eV, such as about 4.61 eV. *See*, e.g., specification at paragraph [0001].

In rejecting the claims, the Examiner refers to col. 2, lines 6-22 to teach a gate electrode comprising a work function close to about a mid-gap of the silicon band gap as claimed. *See* Office Action mailed June 7, 2007 at page 3. Applicants submit that the Examiner has misunderstood the teachings of Bai. In fact, the portion of Bai to which the Examiner refers discusses the problem of mid-gap gate electrodes. To solve this problem, Bai teaches the use of transistors which operate optimally at its respective Fermi level (4.1 eV and 5.1 eV). Operating at the transistor's optimal Fermi level is not the mid-gap level as claimed. *See*, e.g., Bai, Figs. 12-14. Applicants therefore submit that forming a gate conductor having a work function close to about a mid-gap of the silicon band gap is nowhere taught or suggested by Bai.

Also, the Examiner suggests that Bai teaches having all of the first material of the gate material and substantially all of the metal layer over the gate layer are consumed during reaction with one another. To support this position, the Examiner relies on col. 6, lines 51-62 of Bai. Upon closer examination, Applicants submit that the portion of the referred portion of Bai nowhere discusses having all of the first material of the gate material and substantially all of the metal layer over the gate layer are consumed during reaction with one another. It could be that the Examiner may be referring to another portion of Bai which teaches having the polysilicon layer entirely consumed during the reaction. *See* Bai, col. 5 at lines 47-51. However, having the polysilicon layer entirely consumed does not mean that substantially all of the metal layer is consumed. Similarly, providing a gate layer and metal layer having a predetermined ratio which results in the gate material and substantially all of the metal layer over the gate layer are consumed during reaction with one another, as recited by claims 1, 16 and 42, is nowhere taught

or suggested by Bai. Furthermore, Bai nowhere discusses reducing problems associated with inversion and agglomeration during gate formation, as required by claims 16 and 41. Applicants therefore submit that Bai nowhere teaches or suggests the invention as claimed by independent claims 1, 10, 16, 41 and 42.

In rejecting claim 9, the Examiner suggests that Bai inherently teaches substantially all metal material of the metal layer being consumed since Bai teaches that "as much as 5% of the metal" remains after the reaction. To support this position, the Examiner refers to Bai at col. 7, lines 1-5. Applicant submits that Bai nowhere teaches that as much as 5% or substantially all of the metal remains after the reaction. The portion of Bai referred to by the Examiner only states that "unreacted metal layers of Ti and Mo if any such metal remain, are removed by etching" to form complementary "metal gates with work functions of 4.1 and 5.1 electron volt" *See* Bai, col. 7 at lines 1-5.

It is well established that a showing of inherency requires that the missing element or function must necessarily result from the prior art reference. The mere fact that a certain thing may probably or possibly result is insufficient. *See*, e.g., In re Olerich, 666 F.2d 578, 212 USPQ 323 (C.C.P.A. 1981); and In re King, 801 F.2d 1324, 231 USPQ 136 (Fed. Cir. 1986).

Bai teaches that "unreacted metal layers of Ti and Mo, if any such metal remains are removed by etching…." *See* Bai, col. 7 at lines 1-5. The statement only indicates that some metal may remain. For example, this statement would apply to 5%, 10%, 50% or substantially all the metal not being consumed during the reaction. Therefore, Applicants submit that Bai fails to explicitly or inherently teach or suggest the invention as claimed.

Applicants, in view of the arguments presented, submit that claims 1, 10, 16, 41 and 42 are patentable over Bai. Since claims 2-3, 5-9, 11-15, 17-28 and 33-36 are directly or indirectly dependent on claims 1, 10 and 16, these claims are also patentable over Bai. Applicants

therefore respectfully request withdrawal of the rejection to the claims based on 35 U.S.C. 102(b).

Rejection under 35 USC § 103

Claims 22, 26, 31, 35, 39 and 42 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gardner, US 6,100,173 in view of Bai, US 6,204,103. As for the rejection to claims 31 and 39, Applicants submit that this basis of rejection is moot since these claims have been cancelled. With respect to this basis of rejection to the remaining claims, Applicants respectfully disagree.

Gardner describes a silicide process which forms a silicide gate. In the Office Action, the Examiner admits that Gardner "fails to teach the step of processing the metal layer to cause a reaction between the gate layer and the metal layer such that substantially all the material of the gate layer and portions of the metal layer over the gate layer are consumed to form a resulting layer having a work function close to a mid gap of silicon band gap which serves as the gate electrode which contacts the gate dielectrics," as required by claims 16 and 42 *See* Office Action Page 8. The Examiner then relies on Bai to compensate for these defects.

However, as already discussed, Bai fails to teach or suggest the invention as recited by claims 16 and 42. The combination of Gardner fails to compensate for the defects of Bai. Applicants therefore submit that neither Gardner nor Bai, alone or in combination, teaches or suggests providing substantially complete consumption of the material of the gate layer to reduce the problems of agglomeration and inversion. Further, both Gardner and Bai nowhere teach or suggest forming a gate electrode having a work function close to a mid gap of silicon band gap. Therefore, Applicants respectfully submit the claims of the present invention are patentable over

Gardner and Bai, alone or in combination and respectfully request withdrawal of the rejection under 35 U.S.C. §103(a).

Conclusion

In view of the foregoing, Applicants believe that all claims now pending in this Application are in condition for allowance. The issuance of a formal Notice of Allowance at an early date is respectfully requested.

Should the Examiner believe that a telephone conference would expedite prosecution of this Application, please telephone the undersigned attorney at his number set out below.

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Respectfully submitted,

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